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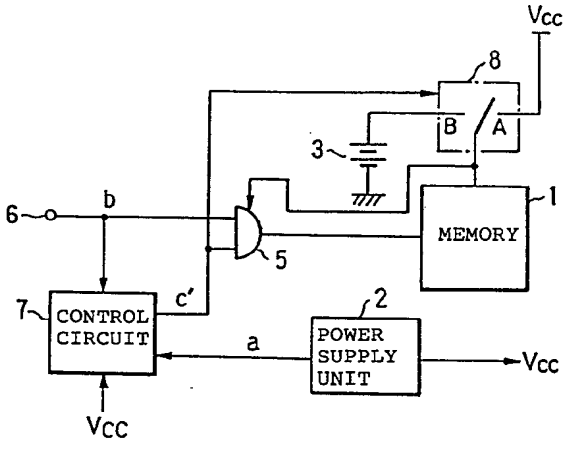
(54) **DATA-HOLDING CIRCUIT IN A MEMORY.**

(57) The invention is to reliably hold the contents stored in a memory even in the power supply interrupt while the memory is being accessed. The circuit of the invention comprises a first detector means (2) which detects the power supply interrupt; a second detector means (7) which detects whether the memory (1) is being accessed or not; a switching means (8) which supplies current from a back-up power supply (3) to the memory (1) only when the power supply interrupt has been detected by the first detector means (2) and the memory (1) that has not been accessed is detected by the second detector means (7); and access inhibit means (5, 7) which inhibit access to the memory (1) only when the power supply interrupt has been detected by the first detector means (2) and the memory that has not been accessed is detected by the second detector means (7); so that access to the memory (1) will not be discontinued before it has been completed.



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S P E C I F I C A T I O N

MEMORY DATA HOLDING CIRCUIT

TECHNICAL FIELD

The present invention relates to a memory data holding circuit which, in case of power supply interruption, supplies as operating current from a backup power supply to a memory to retain its stored data.

BACKGROUND ART

A device using a memory is sometimes provided with a data holding circuit which, in case of power source interruption, supplies an operating current from a backup power supply to the memory, preventing destruction of its stored data.

Fig. 5 illustrates in block form an example of a conventional data holding circuit. Reference numeral 1 indicates a memory such as a C-MOS-RAM or the like, 2 a power supply unit which supplies an operating voltage V_{CC} to each part of the device and yields a detecting signal a which goes to a "1" in the power-ON state and a "0" in the power-OFF state, 3 a backup power supply, 4 a changeover switch which is connected to the side of a contact A or B depending upon whether the detecting signal a is at the "1" or "0" level, 5 an AND gate and 6 an input terminal for a chip select signal b. Incidentally, the detecting signal a goes to the "1" state a certain elapsed time after the rise of the operating voltage V_{CC} and goes to the "0" state a certain time before the fall

of the operating voltage V_{CC}. The memory 1 is accessible when the chip select signal b is at the "1" level which is applied via the AND gate 5.

While the operating voltage V_{CC} is supplied to each part of the device from the power supply unit 2, the detecting signal a is at "1", so the changeover switch 4 will be connected to the contact A side, through which the operating voltage V_{CC} is provided to the memory 1. Furthermore, since the AND gate 5 is in the ON state in this instance, the chip select signal b will be applied via the AND gate 5 to the memory 1. Moreover, when the power supply is turned OFF, the detecting signal a goes to a "0", so the changeover switch 4 is connected to the contact B side and the backup power supply 3 will provide an operating current to the memory 1, holding its stored contents.

With a view to preventing access to the memory 1 during the power-OFF period, however, the conventional arrangement shown in Fig. 5 is adapted so that the chip select signal b is applied to the memory 1 via the AND gate 5 which is controlled by the detecting signal a. This introduces such defect as follows: That is, if power is disconnected from the device when the chip select signal b is at "1" and data is being written in the memory 1, the AND gate 5 will be turned OFF to discontinue the access to the memory 1 although data is being written therein, so that the contents stored at an address being accessed at that time may sometimes become unidentified.

DISCLOSURE OF THE INVENTION

The present invention is intended to overcome such a defect as mentioned above, and has for its object to ensure holding the stored contents of a memory in case of power disconnection.

The present invention is provided with a first detecting means for detecting the interruption of power supply and a second detecting means for detecting whether the memory is being accessed or not. Only when the first detecting means detects that the power supply is OFF and the second detecting means detects that the memory is not being accessed, the access thereto is prohibited and an operating current is supplied to the memory from a backup power supply. This ensures to retain stored contents of the memory even if the power source is turned OFF when the memory is being accessed.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating an embodiment of the present invention; Fig. 2 is a circuit diagram showing an example of the arrangement of a control circuit; Fig. 3 is a diagram explanatory of operations of the circuits depicted in Figs. 1 and 2; Fig. 4 is a diagram illustrating the principal part of another embodiment of the present invention; and Fig. 5 is a block diagram illustrating a prior art example.

BEST MODE FOR CARRYING OUT THE INVENTION

Fig. 1 illustrates in block form an embodiment of the present invention as being applied to a system in which the

memory 1 is accessible when the chip select signal b is at "1". In Fig. 1 reference numeral 7 indicates a control circuit and 8 a changeover switch which is connected to the contact A or B side depending upon whether an output signal c' of the control circuit 7 is at "1" or "0". The same reference numerals as those in Fig. 4 indicate the same parts. Fig. 2 is a circuit diagram showing an example of the arrangement of the control circuit 7. Reference characters Q1 to Q4 designate transistors, R1 to R7 resistors, IN1 and IN2 input terminals, OUT1 and OUT2 output terminals and V_{BB} an operating voltage from the backup power supply 3. Figs. 3(A) to (I) are diagrams for explaining the operations of the circuits shown in Figs. 1 and 2. The control circuit 7 is supplied at the input terminals IN1 and IN2 with the chip select signal b and the detecting signal a, respectively, and the signal c' derived at the output terminal OUT2 is applied to the AND gate 5 and the changeover switch 4. Incidentally, the AND gate 5 is backed up by a battery, and hence is operable even while the power supply is in the ON state.

Now, assuming that the operating voltage V_{CC} and the chip select signal b vary as shown in Figs. 3(A) and (C), respectively, the detecting signal a available from the power supply unit 2 will go to the "1" state (at times t2 and t7) a certain elapsed time after the rise of the operating voltage V_{CC} (at times t1 and t6) and the "0" state (at times t4 and t8) a certain time before the fall of the operating voltage V_{CC}

(at times t5 and t10) as depicted in Fig. 3(B). The transistor Q1 will be turned ON and OFF in response to the "1" and the "0" state of the chip select signal b as shown in Fig. 3(D). Furthermore, since the detecting signal a is at the "1" level from time t2 to t4 and t7 to t8, the transistor Q2 will be in the ON state from time t2 to t4 and t7 to t8 as shown in Fig. 3(E).

Moreover, the transistor Q3 is supplied at its base with current via either one of the transistors Q1 and Q2 if that one of them is in the ON state, so it will be in the ON state from time t2 to t4 and t7 to t9 as shown in Fig. 3(F). When the transistor Q3 is in the ON state, the transistor Q4 is supplied at its base with current, and hence will be in the ON state from time t2 to t4 and t7 to t9 as depicted in Fig. 3(G). Consequently, the signal c' which is provided at the output terminal OUT2 will be at the "1" level from time t2 to t4 and t7 to t9 as depicted in Fig. 3(H), and the signal c from the output terminal OUT1 will be at the "0" level from time t2 to t4 and t7 to t9 as shown in Fig. 3(I).

Accordingly, when the detecting signal a happens to go to the "0" level at time t4, since the signal c' changes from the "1" to the "0" level at time t4, the AND gate 5 will be turned OFF at time t4 to thereby inhibit access to the memory 1 and, at the same time, the changeover switch 8 will be connected to the contact B side, supplying operating current to the memory 1 from the backup power supply 3. In the case

where the detecting signal a happens to be a "0" at time t8, since the transistor Q3 remains in the ON state until time t9, that is, until the chip select signal b goes to a "0", as shown in Fig. 3(F), the signal c' from the output terminal OUT2 will fall from the "1" to the "0" level at time t9 and the AND gate 5 will be turned OFF at time t9, prohibiting access to the memory 1. At the same time, the changeover switch 8 will be connected to the contact B side, supplying operating current to the memory 1 from the backup power supply 3. In addition, even if the chip select signal b goes to a "1" again afterward, the transistor Q1 will not be turned ON since the transistor Q3 for supplying the base current to the transistor Q1 is already in the OFF state.

That is, the control circuit 7 will immediately make the signal c' a "0" if the detecting signal a goes to the "0" state when the memory 1 is not being accessed (at time t4), and if the detecting signal a goes to the "0" state when the memory 1 is being accessed (at time t8), the control circuit will make the signal c' a "0" upon completion of access to the memory 1 (at time t9). Accordingly, even if the power supply is turned OFF when data is being written in the memory 1, the gate circuit 5 will remain in the ON state until access to the memory 1 is completed, so that the stored contents at the address being accessed at that time will not become unidentified.

While the above embodiment has been described in connection with the case where the present invention is

applied to the system in which the memory 1 is accessed when the chip select signal b is at the "1" level, the invention is applicable as well to a system in which the memory 1 is accessed when the chip select signal b is at the "0" level. In such a case, it is necessary only to provide the chip select signal b via an inverter to the input terminal IN1 of the control circuit 7 and to employ, in place of the AND gate 5, a gate circuit which receives the chip select signal b and the signal c from the output terminal OUT1 of the control circuit 7 and provides an output signal "0" only when the both input signals are at the "0" level. Furthermore, although in the above embodiment it is decided by the chip select signal b whether the memory 1 is being accessed or not, it is also possible, of course, to use a write signal for deciding whether the memory 1 is being accessed or not.

As described above, the present invention is provided with a first detecting means (formed by the power supply unit 2 in the embodiment) for detecting that the power supply is turned OFF, a second detecting means (formed by the transistor Q1, etc. in the embodiment) for detecting whether a memory is being accessed or not, a switching means (formed by the change-over switch 8, the transistor Q3, etc. in the embodiment) for supplying an operating current from a backup power supply when the first detecting means detects that the power supply has been turned OFF and the second detecting means detects that the memory is not being accessed, and an access inhibit

means (formed by the AND gate 5, the transistor Q3, etc. in the embodiment) for inhibiting access to the memory when the first detecting means detects that the power supply has been turned OFF and the second detecting means detects that the memory is not being accessed. Accordingly, the present invention possesses the advantage that even if the power supply is turned OFF when data is being written in the memory, the stored contents at the address being accessed at that time will not become unidentified unlike in the prior art.

C L A I M

A memory data holding circuit which, in case of power supply interruption, supplies an operating current to a memory from a backup power supply, characterized by a first detecting means for detecting that the power supply is turned OFF, a second detecting means for detecting whether the memory is being accessed or not, a switching means for supplying the operating current to the memory from the backup power supply when the first detecting means detects that the power supply has been turned OFF and the second detecting means detects that the memory is not being accessed, and an access inhibit means for inhibiting access to the memory when the first detecting means detects that the power supply has been turned OFF and the second detecting means detects that the memory is not being accessed.

FIG. 1

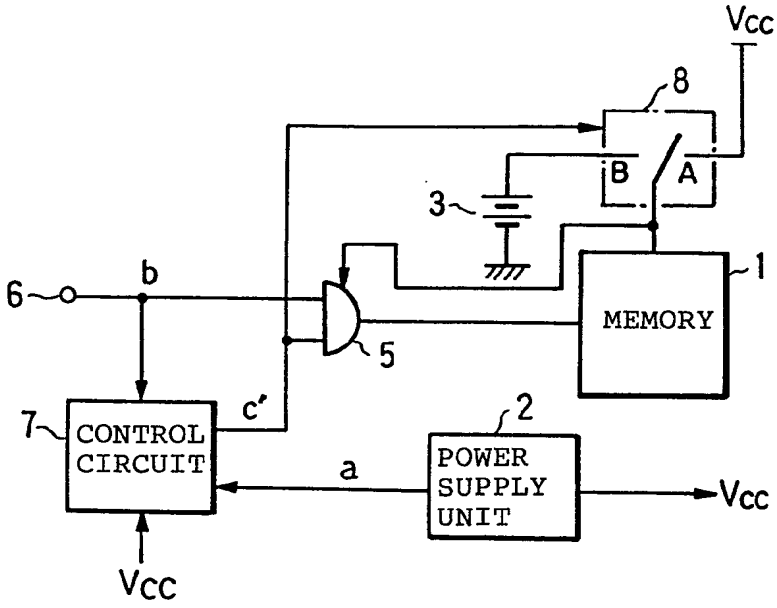
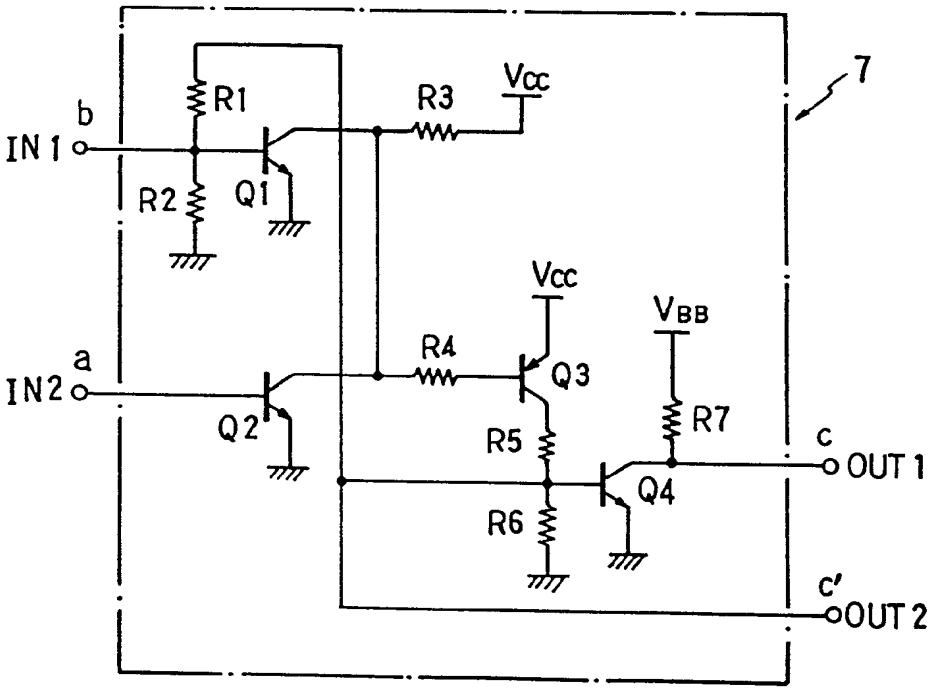

Vcc
8
B
A
3
1
MEMORY
6
b
5
7
CONTROL CIRCUIT
c'
2
POWER SUPPLY UNIT
a
Vcc
Vcc

FIG. 2


7
IN 1
b
R1
R3
Vcc
R2
Q1
IN2
a
Vcc
VBB
R4
Q3
Q2
R5
R7
c
OUT 1
Q4
R6
c'
OUT 2

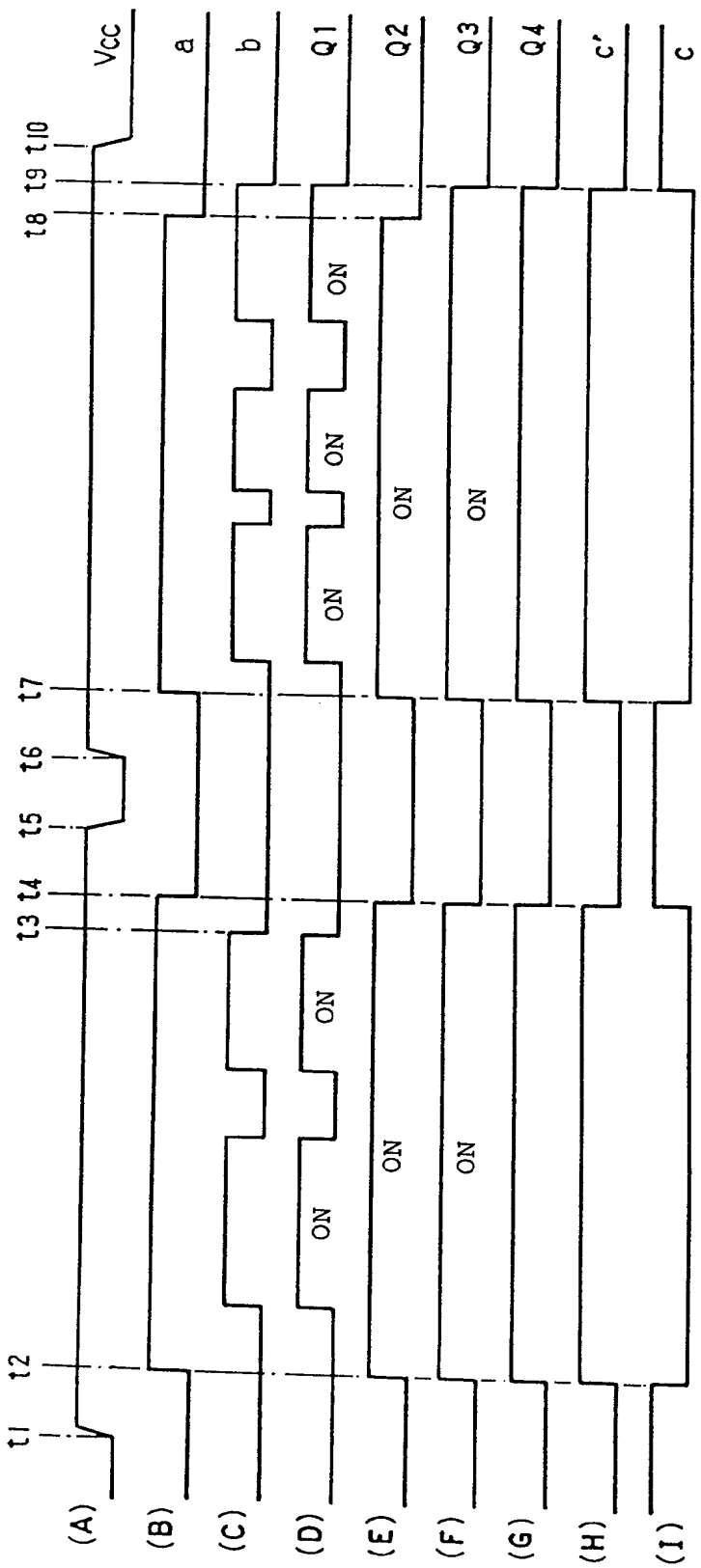


FIG. 3

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FIG. 4

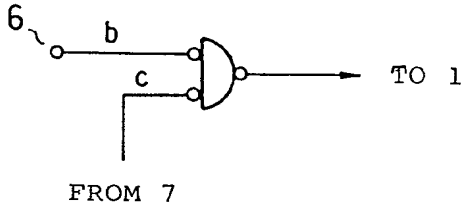
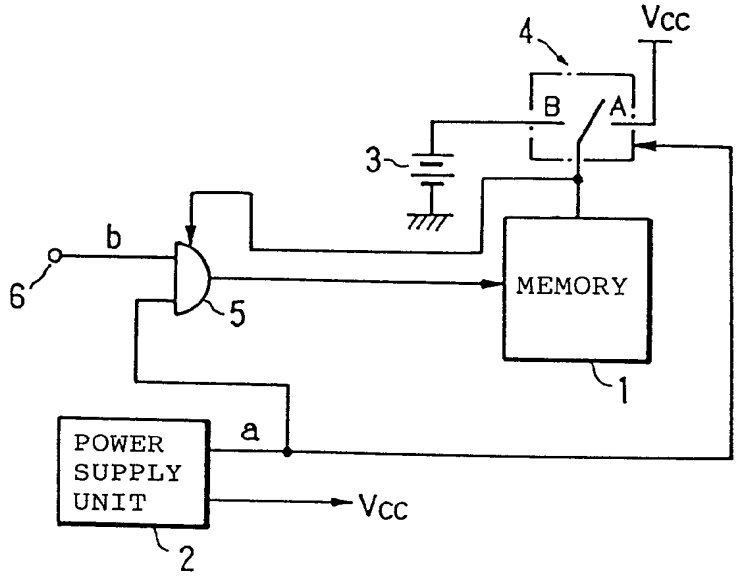


FIG. 5



INTERNATIONAL SEARCH REPORT

0181943

International Application No. PCT/JP85/00263

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[4] G06F1/00, 12/16, G11C11/34

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	G06F1/00, 12/16, G11C11/34

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

Jitsuyo Shinan Koho	1971 - 1984
Kokai Jitsuyo Shinan Koho	1971 - 1984

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category*	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	JP, A, 58-100300 (Hitachi, Ltd.) 14 June 1983 (14. 06. 83) (Family : none)	1
Y	JP, A, 53-76715 (Hitachi, Ltd.) 7 July 1978 (07. 07. 78) (Family : none)	1
Y	JP, B1, 43-15100 (Fuse Air Craft Company) 25 June 1968 (25. 06. 68) Column 3, lines 36 to 44 (Family : none)	1

* Special categories of cited documents: [15]

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"P" document published prior to the international filing date but later than the priority date claimed

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
August 1, 1985 (01. 08. 85)	August 12, 1985 (12. 08. 85)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
Japanese Patent Office	